IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) A timing generation circuit comprising:

a timing memory containing predetermined timing data; ~~and~~

a counter for loading timing data output from the timing memory and outputting a pulse signal at a timing indicated by the timing data~~,~~; and

~~the timing generation circuit further comprising~~ load data switching means for dividing a memory region of the timing memory, selecting one or a plurality of timing data output from the divided memory regions, and loading the selected one or plurality of timing data in the counter to thereby output the pulse signal of one timing indicated by the one or plurality of timing data;

wherein the load data switching means divides the timing memory into a plurality of memory regions either in a column direction or a row direction to generate the plurality of timing data at the same time.

2. (currently amended) The timing generation circuit according to claim 1, wherein the load data switching means divides the memory region of the timing memory in ~~by~~ the column direction which is an address direction of the timing memory in response to switching of a mode signal, links ~~a~~ the plurality of timing data output from the divided memory regions in the row direction which

is a data bit width direction of the timing memory, and loads these data as one timing data in the counter.

3. (currently amended) The timing generation circuit according to claim 1, wherein the load data switching means comprises:

an address selection circuit which designates one or a plurality of addresses of the timing memory by switching of a mode signal and which outputs one or a plurality of timing data stored in the corresponding one or plurality of addresses; and

a load data switching circuit which loads the one timing data as ~~such~~ is in one counter, when one timing data is output from the timing memory by the switching, and which loads the plurality of timing data in a plurality of cascaded counters, when a plurality of timing data are output from the timing memory by the switching, to thereby output the pulse signal of one timing indicated by the one or plurality of timing data.

4. (currently amended) The timing generation circuit according to claim 3, wherein the address selection circuit divides one designated address by the switching to thereby designate N (N is a natural number) addresses, and outputs N timing data from the timing memory, and

the load switching circuit loads the N timing data in N cascaded counters by the switching to thereby output the pulse signal of one timing indicated by the N timing data.

5. (currently amended) The timing generation circuit according to claim 1, wherein the load data switching means divides the memory region of the timing memory in the row direction which is a data bit width direction ~~by~~ of the timing memory in response to switching of a mode signal, selects one timing data from the respective timing data output from the divided memory regions, and loads the data in the counter.

6. (currently amended) The timing generation circuit according to claim 1, wherein the load data switching means comprises:

a data division circuit which divides the timing data stored in one address of the designated timing memory into a plurality of timing data and which outputs the plurality of divided timing data ~~by~~ in response to switching of a mode signal or which outputs one timing data among the plurality of divided timing data; and

a load data switching circuit which loads the plurality of timing data in a plurality of cascaded counters, when the plurality of divided timing data are output from the timing memory by the switching, and which loads the one timing data as such in one counter, when one divided timing data is output from the timing memory by the switching, to thereby output a pulse signal of one timing indicated by the plurality of or one divided timing data.

7. (currently amended) The timing generation circuit according to claim 6, wherein the data division circuit divides one

timing data stored in one designated address into N timing data, inputs the timing data, and further designates and outputs some or all of the N divided timing data, and

the load switching circuit loads the N divided timing data in the corresponding N counters, and thereby outputs a pulse signal of the timing indicated by N timing data per address.

8. (currently amended) A semiconductor test device, which inputs a predetermined test pattern signal into a device under test constituting a test object and which compares a response output signal output from this device under test with a predetermined expected pattern signal to thereby judge whether or not the device under test is satisfactory, the semiconductor test device further comprising:

a timing generation circuit which outputs a reference clock signal of the test pattern signal as a delay clock signal delayed by a predetermined time,

the timing generation circuit comprising: ~~the timing generation circuit according to claim 1~~

a timing memory containing predetermined timing data;

a counter for loading timing data output from the timing memory and outputting a pulse signal at a timing indicated by the timing data; and

load data switching means for dividing a memory region of the timing memory, selecting one or a plurality of timing data output from the divided memory regions,

and loading the selected one or plurality of timing data in the counter to thereby output the pulse signal of one timing indicated by the one or plurality of timing data;

wherein the load data switching means divides the timing memory into a plurality of memory regions either in a column direction or a row direction to generate the plurality of timing data at the same time.